New boundary scan paradigm provides virtual access to circuit boards for real-time manual fault diagnosis and stimulus generation.

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ABSTRACT

IEEE Std 1149.1 has enjoyed tremendous success in both IC Manufacturing and large-scale board assembly facilities. The benefits of boundary scan are fully understood and adopted by these industry segments. Boundary scan tools available for circuit card assembly fault-analysis are mature and well integrated into the test flow in these applications. Unfortunately, outside of these tight communities, boundary scan is still largely unknown and not well understood. It is only relatively recently that boundary scan has become available in focused applications such as FPGA downloading and CPLD programming.

Based on work initiated within the GA Tech School of Electrical and Computer Engineering, a new engine has been developed which removes the tedium normally associated with the use of boundary scan. This engine has been wrapped in a user interface which simplifies boundary scan to the point that any bench technician and/or circuit board designer can easily scan a board with little or no formal instruction.

The user interface parses user selected BSDL files, builds a virtual part that is placed on the screen and then automatically connects the part into the scan chain. The user simply presses “scan” and instantly sees activity on every scan-enabled pin on every device in the chain, in real time on the screen – as provided by the SAMPLE/PRELOAD functionality of IEEE 1149.1. The tool also provides point and click access to the EXTEST functionality of every pin on the device.

The paradigm is extended by providing virtual indicators and controls that the user can “connect” to any scan-enabled pin to monitor the status of the pin and control the operation of the pin. These indicators and controls are presented as familiar LED’s and simple switches to aid in the adoption and acceptance of the virtual test methodology.

The benefits of this new paradigm are three-fold. First, a useful tool is created that provides visibility and control over otherwise inaccessible test points on a circuit card. This helps solve a problem with the adoption of new packaging technologies – engineers are reluctant to use packages that inhibit or prevent the use of traditional test equipment. Packages such as BGA’s do not allow access to pins. This frustrates designers and technicians who are trying to debug circuit cards. Full automatic traditional boundary scan solves this problem, but it is not typically available to designers in lab environments due to high cost and complexity. This new boundary scan technology presents the information in a simple intuitive manner that is already familiar to the user without the need for the traditional test equipment.

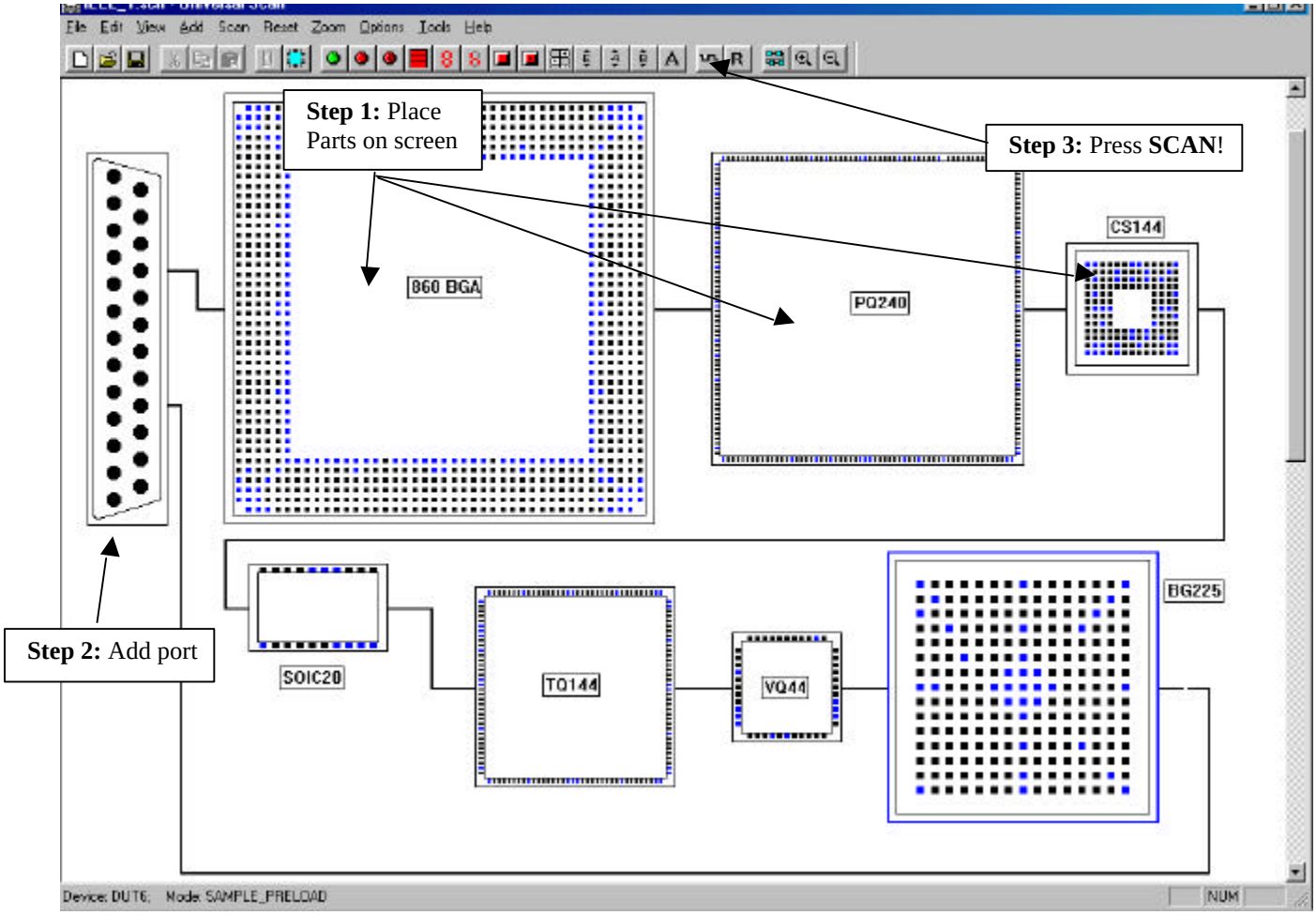
A second benefit is that this new point-n-click approach to boundary scan makes the technology more approachable, which provides engineers and technicians the opportunity to learn about the benefits of boundary scan. After seeing boundary scan in action at a low/manual level the designers will now have a fundamental understanding of the test technology. This in turn will then be reflected in future designs, which will aide in the overall testability of circuit cards in general.

The third benefit is cost. One of the biggest impediments to acceptance of boundary scan by the general design and test community has been cost. Entry level systems appear to be too expensive to anyone that does not understand the benefits of the technology. While this paradigm does not provide the same level of functionality as traditional boundary scan test systems, it does a tremendous job of educating day to day

designers so they can understand the power of boundary scan and can justify the purchase of the tools needed to do the job.

VIRTUAL ACCESS VIA SAMPLE-PRELOAD

In an effort to bring Boundary Scan down to a level that the average design engineer and technician could use, this tool employs a Virtual Package model. The user simply places the package(s) on the screen, "connects" them to a port on the computer, and presses the Scan button, as shown below:



Upon pressing the SCAN button, each of the virtual pins blinks as if is an LED had been connected to every pin on the device. The user can now "see" activity on every pin on every device in the scan chain. This is especially helpful when trying to determine if an oscillator is connected to a pin buried under an otherwise inaccessible BGA package, for example. Or, for viewing an address or data bus to see if any of the address/data lines are active or stuck at a particular value. Since this is SAMPLE/PRELOAD boundary scan information that is being displayed, the user is actually looking at the signals *inside* of the integrated circuit, which ensures the true connectivity across the solder joint.

In addition, the user can specify which scan cell should be viewed on a pin by pin basis. The INPUT cell, OUTPUT cell and TRISTATE cell can be viewed simply by toggling the state of the pin. Normally the INPUT cell is preferred since it displays what is seen at the physical pin on the device.

Pins can also be color coded to highlight functionality or to visually indicate which scan cell is being viewed.

An additional benefit of the viewing the activity of virtual pins is there is no longer any potential for shorting pins together with a scope probe or damaging the solder connection of the pin (for those parts where the pins are accessible, of course!).

AUGMENTING VIRTUAL ACCESS

While viewing the activity on virtual pins is a very powerful debug tool, it is not terribly convenient when groups of signals (address and data busses, for example) are spread amongst the pins on multiple JTAG devices.

To help simplify and organize the signals being viewed, the tool provides virtual indicators in various shapes, sizes and form factors. These indicators appear as simple LEDs, bar graph LEDs, 7-Segment LEDs, etc and can be connected to any pin on any device.

Using the virtual indicators, common signals can be grouped and displayed in a convenient easy to view fashion. Each indicator can also be color coded and inverted to aide the organization of the signals.

The use of these virtual indicators provides a simple intuitive user interface that is instantly recognizable to any design engineer and technician. This expedites the learning curve and eases adoption of the technology.

All of these indicators just provide a visual way of extracting data from the TDO output data and displaying it for the user.

The user can also provide net names for each pin as aliases, which can be used to display information about the device, instead of having to remember the pin name, associated with each signal.

VIRTUAL CONTROL VIA EXTEST

Viewing the status of the IC pins in real time is a tremendous asset – especially for pins that are otherwise inaccessible like those under a BGA package or fine pitch parts that are difficult to reach. The real power of boundary scan, and therefore this tool, is the ability to sever the connection between the internal logic and the external pins and the ability to take control of the pins and drive them to any arbitrary state.

This tool takes standard boundary scan EXTEST techniques and wraps a simple user interface around it to provide total control of each and every scan-enabled pin in the JTAG chain. With this tool, the user toggles the device into EXTEST mode and then simply changes the state of the pin with a point-and-click of the mouse.

This allows the user to manually force any pin to any state at any time. Warnings are provided to remind the user that placing the device in EXTEST can be dangerous since they now have total unrestrained control of the output drivers on the pins. This is important to help prevent the user from accidentally driving pins that should not be driven.

This is similar to the “old days” when we would grab any piece of metal and manually short a pin to VCC or GND to see what would happen. The difference is that with boundary scan there is no danger of accidentally shorting adjacent pins and with today’s newer packages you couldn’t get to the pins if you wanted to. Also, with boundary scan you are controlling the output driver, not fighting it.

It is important to note that via boundary scan this tool allows the users to not only toggle the state of the output driver, but it also allows them to toggle the state of the Tri-State control. This can be an invaluable debug tool when things are not going according to plan.

AUGMENTING VIRTUAL CONTROL

While manual control of the pins provides another powerful debug tool, it can get tedious locating each pin and then toggling it by clicking on the mouse.

Virtual Switches are provided to help the user organize and control the pins under EXTEST control. The user simply "connects" a switch to each pin to be controlled, and then toggles the switch to control the pin. Each time a switch is pressed, the tool simply places the associated value in the TDI input stream to be processed on the next scan iteration.

The switch paradigm provides a very familiar and intuitive interface for the user. This in turn helps lower the barriers to using EXTEST and boundary scan and makes it simple to manually test and control signals or groups of signals. The tool provides toggle switches, momentary switches, hex thumbwheel switches, DIP switches, 7-Segment control Switches, etc.

PUTTING IT AL TOGETHER

Given the ability to manually monitor and control pins via an intuitive interface, it becomes a simple matter to build a small control panel that can be used to test circuit cards. This control panel can be saved to disk for future reference and even be used in limited prototype and production runs of small quantities of boards.

To extend this even farther, if the user has the foresight to bring the JTAG control signals out to a test connector on the exterior of the system, the user can then monitor and control the system without ever removing the covers on the box or even having to physically see the circuit under test. This can be an invaluable asset when the software folks are saying the hardware is failing and the hardware folks are saying the software is the problem. Boundary scan places the tester exactly between these two by providing visibility into exactly what is going on INDEPENDENT of either. The tester can drive the hardware to see if it is functioning and can view the pin activity to see if the software is actually trying to drive it.

This is also particularly useful during initial board assembly and debug. By using boundary scan, this tool allows the user to validate continuity and even test hardware functionality BEFORE the FPGA or PLD or Microprocessor is programmed! While this is not news to anyone who is familiar with traditional boundary scan debug tools, it is very new and novel to the scores of bench designers and technicians that have never had access to this powerful functionality before.

DUT PROPERTIES VISIBILITY

The IC's that are placed on the display are generated from the manufacturer's BSDL files. There is a tremendous amount of information about the part in these BSDL files that this tool makes available to the user via simple dialog boxes. Part pinout can be viewed and even sorted. Global properties can be changed and design warnings can be viewed. The tool also provides a BSDL file viewer in case anyone wants to quickly view the source of the part.

This provides a handy reference for the user, but it also helps aid in the understanding of boundary scan in general.

INCREASING BOUNDARY SCAN AWARENESS

We have begun market trials of this new technology in the southeastern US. The feedback has been extremely positive on two fronts. First, designers are thrilled to finally have this kind of manual access and visibility to help them debug circuits. Second, they appreciate the educational value of this tool. We have

yet to meet a single design engineer, FAE or technician that actually understood what boundary scan was until they saw this tool in action.

This in turn serves as a stepping stone up to the more powerful automatic JTAG tools already available on the market today. Until now, it was hard to justify the expense because the average designer and technician didn't understand what boundary scan was all about. This tool compliments existing technologies, it does not pretend to replace them.

STANDARDIZATION

The Achilles heal of boundary scan has been lack of high quality reliable BSDL files and simple inexpensive tools that allow users to take advantage of them. Most manufacturers have addressed the first issue and this tool addresses the second issue.

Unfortunately, one of the areas lagging in the manufacturer's adoption of the BSDL file structure is the consistency of the package names. Each manufacturer has their own preferred naming convention for a given package style and this is reflected in the BSDL files. Some manufacturers don't put any package style in the BSDL files.

Technology such as the tool described in this paper rely heavily on clear concise standardized definition of the package type in the BSDL files. Until package naming is standardized, it will be difficult to advance technologies such as this. It is very difficult to keep up with the myriad of package styles that exist and all of the new ones that are continuously being introduced into the market as we continue our push towards higher and higher board densities and reduced pack sizes.

SUMMARY

This paper demonstrates a new way of looking at boundary scan and introduces a new tool that is useful and educational. The tool promotes the use of Boundary Scan and makes it easier to justify the use of high-density packages (most engineers avoid these due to the inaccessibility of the pins). The simple user interface and low cost assist the adoption of boundary scan and raise the awareness among the design community.