Got the BGA Blues?

Learn how to obtain visibility into the pins of a ball grid array package using Boundary Scan and the Universal Scan debugging tool.

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The first prototype of a board populated with BGAs returns from assembly. You attach the Xilinx download cable, apply power, attempt to download test data, and you get – nothing. Debugging is easy when you have access to signal pins – but this board has BGAs, so you can't probe the pins effectively. You wish you could:

- Monitor how mode-select pins are set
- Check continuity across BGA solder connections
- See if the oscillator is connected to the part
- Check the DIN/DONE/CCLK line continuity
- See if the data/address or other signals are active or connected to the part.

It would be wonderful if you could peel the chip open. But you can't. There are, however, more sophisticated ways to access BGA pins. This article introduces Universal Scan™ – a new tool that takes advantage of IEEE 1149.1 Boundary Scan, commonly known as JTAG, a feature already built into every Xilinx device. It provides visibility and control over the pins under that BGA – or any JTAG device – quickly, easily, and inexpensively.

JTAG Background – The Basics

You are probably already familiar with the JTAG interface – TCK, TDI, TDO, and TMS – and how JTAG is used to configure Xilinx devices. You may not be as familiar with Boundary Scan, another powerful test technology.

Boundary Scan Overview

Understanding and using Boundary Scan requires only three basic pieces of information:

- **How the scan chain is connected** – Where does Boundary Scan reside inside your Xilinx device?
- **How the scan cells are connected** – How does Boundary Scan interface with your signals?
- **Boundary Scan operational modes** – What are they and how do they affect the scan cells and the information you can access?

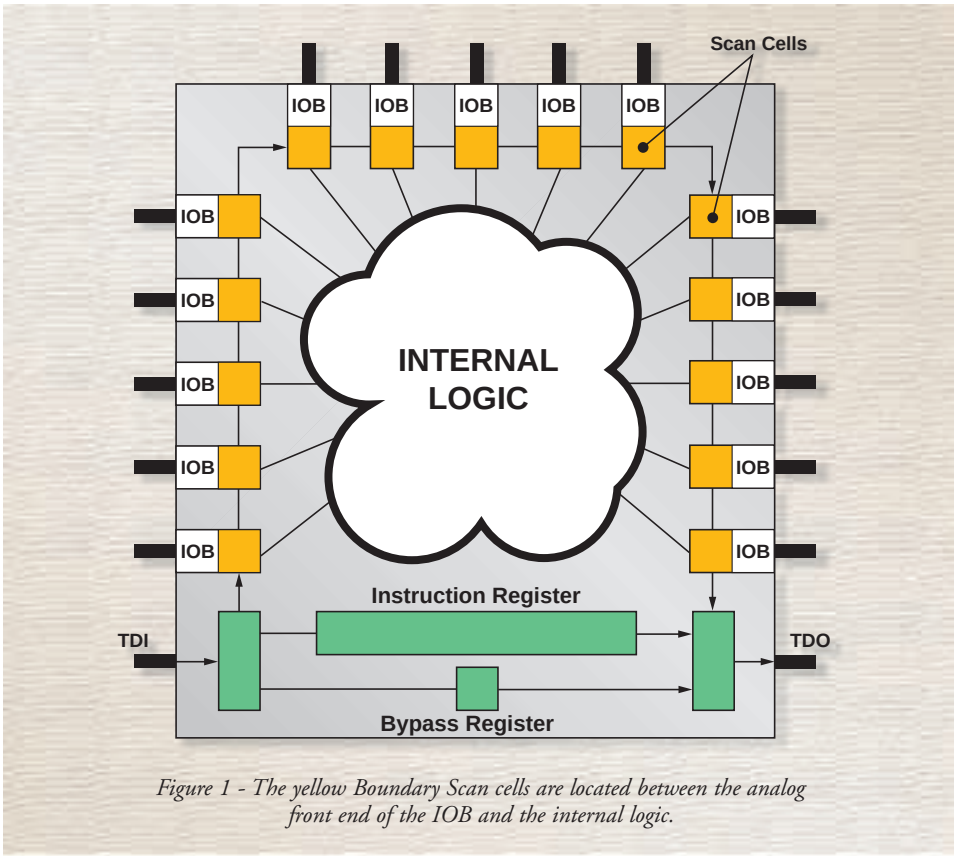

Figure 1 - The yellow Boundary Scan cells are located between the analog front end of the IOB and the internal logic.

The Scan Chain

At the most fundamental level, Boundary Scan is illustrated in Figure 1. Logic occupies the interior of the device. Pins occupy the perimeter, or boundary. The interconnects between each pin and the internal logic pass through the Boundary Scan logic blocks (yellow in Figure 1). Boundary Scan blocks are on the logic side of the IOB (input/output block). They are normally transparent to the operation of the device; signals flow unimpeded through them.

Each of these blocks is connected around the boundary of the part to form a giant shift register (the boundary register). When in Boundary Scan mode, TDI is connected to one end of the shift register, and TDO is connected to the other end. TCK and TMS are used to shift data in and out of this giant shift register.

TDI and TDO can be connected to numerous registers (such as those used to configure the part). Two of the registers are shown in Figure 1: the instruction register and the bypass register.

To use Boundary Scan, you simply shift an instruction into the instruction register and then shift data in/out of the associated data register.

The bypass register is used to skip over a part in a scan chain. Skipping parts of the scan chain allows you to bypass the boundary register and exit in a single TCK cycle.

Scan logic in each of the scan cells consists of a group of registers that captures the state of signals entering and exiting the device, and a group of registers that can drive these same signals. The operation of these cells depends on the Boundary Scan mode.

Manufacturers may define many Boundary Scan modes for a given device, but only the three required by the IEEE 1149.1 standard are necessary for successful debugging. These modes are: SAMPLE/PRELOAD, EXTEST, and BYPASS.

SAMPLE PRELOAD

In the SAMPLE/PRELOAD mode of Boundary Scan, the logic inside the yellow

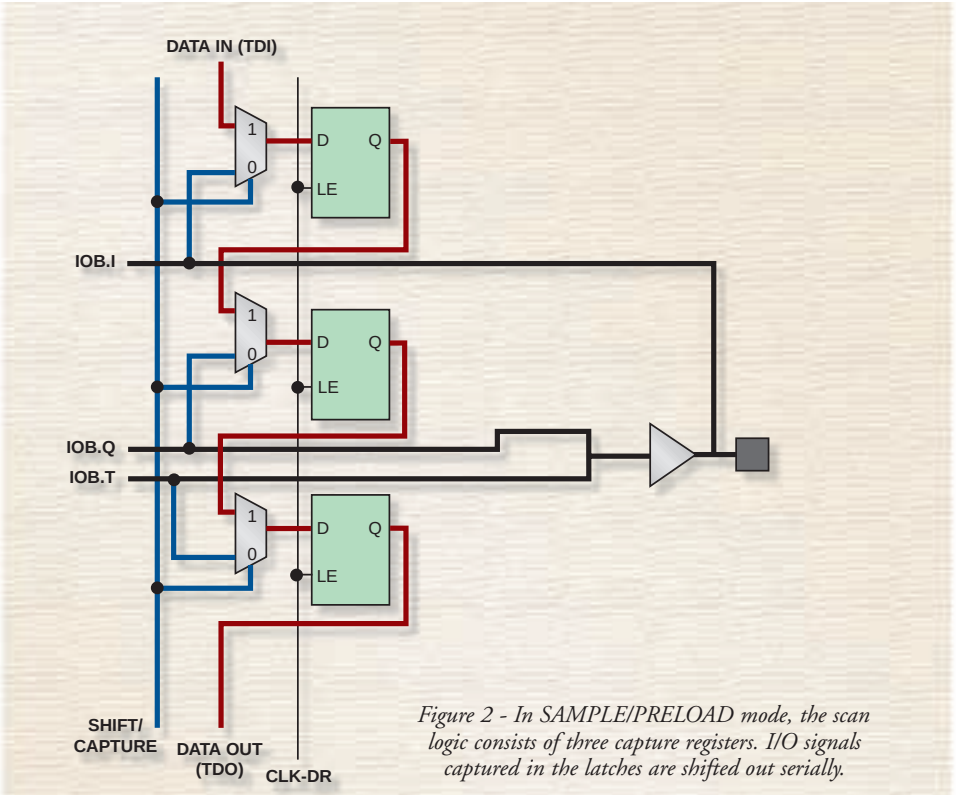

Figure 2 - In SAMPLE/PRELOAD mode, the scan logic consists of three capture registers. I/O signals captured in the latches are shifted out serially.

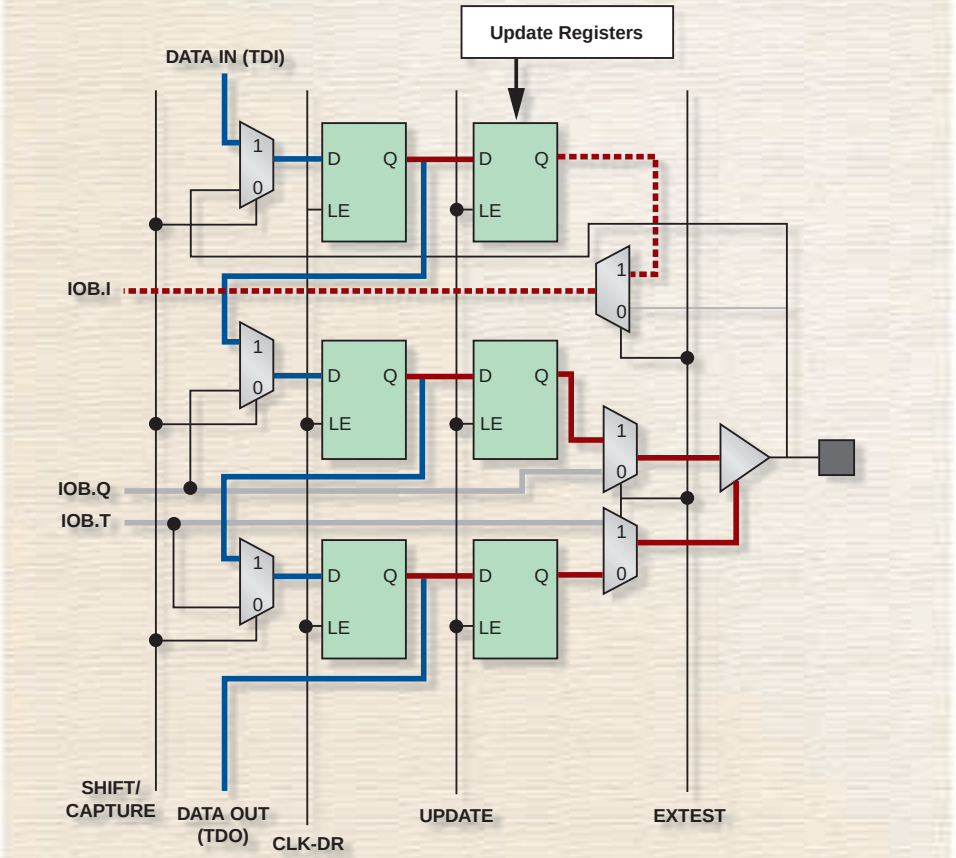

Figure 3 - In EXTEST mode, normal signal flow is interrupted and data that had been shifted into the update registers by the test engineer is applied to the signals.

blocks of Figure 1 is represented in greater detail in Figure 2.

One capture register is dedicated to each signal typically associated with an I/O buffer (INPUT, OUTPUT, TRISTATE). On a command set by the test engineer, these registers, or scan cells, capture the state of all three signals (or however many there are for the pin). Once data is captured, it is shifted out (the red path in Figure 3), and the state of the pin is displayed. Data can be captured at any time. It is asynchronous with signals flowing in and out of the device. The capture process does not interfere with the circuit's operation.

EXTEST

When a part is in EXTEST mode, data that the test engineer wants to apply to the OUTPUT, TRISTATE – and in some cases, INPUT – signals is shifted into the scan chain. Although the capture registers from SAMPLE/PRELOAD still capture the states of the signals flowing through the device, they never go anywhere. The signals are cut off from their normal function and the data shifted into the update registers is applied to the signals, as shown in Figure 3. Captured data is shifted out as update data is shifted in.

BYPASS

We have already touched on BYPASS. In this mode, the Boundary Scan chain is bypassed and all TDI data flows through the part in one TCK cycle.

Applying Boundary Scan to Access Pins

Using the JTAG state machine to implement Boundary Scan can be tedious. But the new Universal Scan debug tool from Ricreations Inc. automates much of the work. You simply drop virtual parts on the screen, connect the JTAG signals to the parallel port, and hit the SCAN button. Instantly, the activity of every pin under the BGA (or around any JTAG part) appears on your PC display.

Each of the red or black dots in Figure 4 represents a pin. Red represents a logic High; black a logic Low. Blue is a pin that can't be scanned (power, ground, and such).

If a pin is toggling, that means there is signal activity on that pin. Typically, this is all we want to know when we use an oscilloscope to debug – whether the pin is high, low, or toggling. The Universal Scan tool is an activity indicator. You instantly see – in real time – if the mode select pins are set correctly, if the oscillator is connected, if the data bus or address bus is active, and so on.

Universal Scan software does not require netlists, test executives, test fixtures, or other board-test peripherals. You don't have to maintain a parts library, because the Universal Scan program doesn't need it. You simply supply the BSDL files, which are freely available from vendor websites, and the Universal Scan tool builds a virtual part on the fly. All that is required is a JTAG-enabled part; packaging doesn't matter.

A valuable aspect of Boundary Scan testing is that, while in SAMPLE/PRELOAD mode, you can monitor all the pins while your circuit is running at full speed without any impact on the system. SAMPLE/PRELOAD mode is completely transparent to the system. How often have you touched an oscilloscope probe to a pin only to create probe loading that changes the circuit's operation, especially with new high-speed circuits? Boundary Scan does not have that problem – it is completely unobtrusive.

Because watching pins blink on the screen can be tedious, the Universal Scan screen display offers virtual indicators (LEDs) that you connect to the pins to organize those aspects of the circuit's activity that interest you. It also has virtual switches that allow you to manually drive a pin to a known state.

To perform a continuity test between two devices, put one device into EXTEST mode and toggle the virtual switches connected the output buffers. The LEDs connected to the other device's input buffers will show the result. Performing a continuity test this way is quick, easy, and does not require touching the board.

To monitor results on an oscilloscope, you can drive signals from the BGA to a connector. This gives total visibility and control over every scan-enabled pin on the part. You are only limited by your imagination.

Because Boundary Scan is independent of internal activity, the part does not have to be configured for this testing. You can take the board right off the factory floor and start testing it before the VHDL/Verilog/firmware is ready.

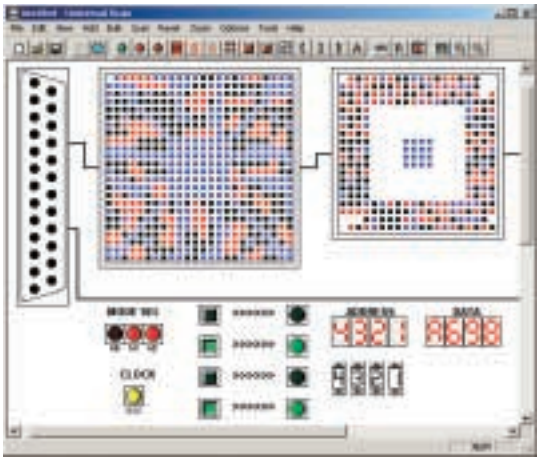

Figure 4 - Virtual switches and LEDs help organize and control the pin information.

Conclusion

Using Boundary Scans to probe otherwise inaccessible pins under a BGA is an easy, three-step process with the Universal Scan tool:

1. Drag and drop the parts under test on the PC screen.
2. Connect the JTAG chain to the parallel port.
3. Hit the Scan button.

Instantly you can monitor the activity of every JTAG-enabled BGA pin (or around any scan-enabled device) on your PC display.

You don't need test fixtures, netlists, or test executives. The devices don't have to be configured. You can start testing the board right off the factory floor before the firmware is complete.

You'll find information on the Universal Scan toolset on the *www.xilinx.com* website by following this click chain: *Products/System Resources/Configuration Solutions/Third-Party Tools/Universal Scan.* Or you can go directly to *www.UniversalScan.com.* Σ